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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/744,522	01/25/2001	Peter Haas	P00,1963	8561
<div>7590 06/08/2007 KEVIN R. SPIVAK MORRISON & FOERSTER LLP 2000 PENNSYLVANIA AVENUE ,NW WASHINGTON, DC 20006-1888</div>			<div>EXAMINER PRICE, NATHAN E</div>	
			<div>ART UNIT 2194</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 06/08/2007</div>	<div>DELIVERY MODE PAPER</div>

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/744,522

Applicant(s)

HAAS, PETER

Examiner

Nathan Price

Art Unit

2194

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is in response to communications received 20 March 2007.

Claims 10 – 20 are pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that the disclosed byte swapping is not a conversion as claimed.

Examiner respectfully disagrees. Lee states that the byte swapping is a conversion [col.

3 lines 53 – 57] and is based on address information [col. 3 line 62 – col. 4 line 3].

Saunty also teaches an object-oriented data conversion unit that performs byte swapping [col. 3 lines 8 – 16]. Ronen was not relied upon to reject the limitations addressed in Applicant's arguments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. Claims 10 – 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Pat. 5,828,884; hereinafter Lee) in view of Sauntry et al. (US 6,349,344 B1; hereinafter Sauntry).

4. As to claim 10, Lee teaches a hardware architecture for a core of a processor [col. 6 lines 39 – 41], comprising:

at least one unit for executing one of a logical or arithmetic operation [Fig. 5, processor 510]; and

a data conversion unit for recognizing a type of data and a data address [col. 3 lines 53 – 67], for external data [col. 3 lines 63 – 64], the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation [col. 3 lines 53 – 67], whereby the data conversion unit recognizes a type of data based upon a type of information accompanying the data address and matches the type of data and the data address before one of an operation is performed or a predetermined type of data is generated in the event of non-match [abstract; col. 3 line 53 – col. 4 line 3].

5. Lee fails to specifically teach an object-oriented data conversion unit. However, Sauntry teaches an object-oriented data conversion unit [col. 3 lines 8 – 16]. It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Sauntry teaches that Java components

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sometimes need to be converted between endian formats [col. 2 lines 18 – 29] and Lee teaches performing the conversion between endian formats [col. 3 lines 53 – 67].

6. As to claim 11, Lee modified by Saunty teaches a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area [col. 3 line 62 – col. 4 line 3; col. 4 lines 16 – 27; col. 5 lines 60 – 62].

7. As to claim 12, Lee modified by Saunty teaches the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation [col. 3 lines 57 – 62].

8. As to claim 13, Lee modified by Saunty teaches the object-oriented data conversion unit is arranged to precede storing of the object in an external storage and a register file [col. 3 lines 57 – 62; col. 5 lines 60 – 62; col. 9 lines 28 – 35].

9. As to claim 14, Lee teaches a register file is divided into a memory area for data and a memory area for a respective type indication of the data [col. 3 lines 62 – 67; col. 4 lines 10 – 15; col. 9 lines 28 – 35].

10. As to claim 17, Lee teaches a method for data conversion in a processor having at least one unit, the method comprising the steps of:

executing a logical or arithmetic operation in the processor [col. 6 line 64 – col. 7 line 18];

implementing a data conversion by a type information in an address and by a type information of the data [col. 3 line 62 – col. 4 line 15];

generating an inequality of the data to be operated by the logical or arithmetic operation based upon the type of data matched to one another or a predetermined data type of data [col. 3 line 62 – col. 4 line 15; col. 8 lines 7 – 15]

11. Lee fails to specifically teach an object-oriented data conversion unit. However, Sauntry teaches an object-oriented data conversion unit [col. 3 lines 8 – 16]. It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because Sauntry teaches that Java components sometimes need to be converted between endian formats [col. 2 lines 18 – 29] and Lee teaches performing the conversion between endian formats [col. 3 lines 53 – 67].

12. As to claim 18, Lee teaches:

dividing a memory location for an object address and a memory location of a register into a first and second area [col. 3 line 62 – col. 4 line 3; col. 4 lines 16 – 38; col. 9 lines 30 – 35] and type information of a memory address deposited in the second area of the object address [col. 4 lines 28 – 38]; and

noting the data of the register deposited in the second area in the first area [col. 4 lines 16 – 27].

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13. Claims 15, 16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Sauntry as applied to claims 10 and 17 above, and further in view of Ronen (US Pat. 5,701,442).

14. As to claims 15, 16, 19 and 20, Lee fails to specifically teach RISC or CISC processors. However, Ronen teaches the use of RISC and CISC processors [col. 6 lines 57 – 60] with a computer designed to provide increased compatibility for systems, including compatibility regarding big and little endian formats [col. 3 lines 35 – 38], which is taught by Lee. It would have been obvious to one of ordinary skill in the art at the time Applicant's invention was made to combine these teachings because both Lee and Ronen teach systems designed to provide compatibility for different endian formats.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan Price whose telephone number is (571) 272-4196. The examiner can normally be reached on 6:30am - 3:00pm, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on (571) 272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NP